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PATENT APPLICATION

ATTORNEY DOCKET NO. 200301967-2

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Andrej Kocev et al.

Confirmation No.: 1813

Application No.: 09/944,776

Examiner: Pham, Thomas K.

Filing Date: 08/31/2001

Group Art Unit: 2121

Title: PROGRAMMABLE TUNING FOR FLOW CONTROL AND SUPPORT FOR CPU HOT PLUG

Mail Stop Appeal Brief-Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF REPLY BRIEF

Sir:

Transmitted herewith in ***triplicate*** is the Reply Brief with respect to the Examiner's Answer mailed on **March 24, 2006**. This Reply Brief is being filed pursuant to 37 CFR 1.193(b) within two months of the date of the Examiner's Answer.

(Note: Extensions of time are not allowed under 37 CFR 1.136(a))

(Note: Failure to file a Reply Brief will result in dismissal of the Appeal as to the claims made subject to an expressly stated new grounds of rejection.)

No fee is required for filing of this Reply Brief.

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Number of pages: **6**

Typed Name: **Melissa Altman**

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Respectfully submitted,

Andrej Kocev et al.

By _____

Michael R. Reinemann

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re The Application of:
Andrej Kocev et al.

Serial No.: 09/944,776

Filed: August 31, 2001

For: Programmable Tuning for Flow Control and Support for CPU Hot Plug

Examiner: Pham, Thomas K.

Art Unit: 2121

Cesari and McKenna, LLP
88 Black Falcon Avenue
Boston, MA 02210
May 19, 2006

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Melissa Altman

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPLY BRIEF

In response to the Examiner's Answer mailed March 24, 2006, Applicants hereby submit this Reply Brief.

ARGUMENT

The Examiner's Answer includes several new grounds of rejection at pp. 16-20, which is the section of the Answer responding to the arguments raised in the Applicants' Appeal Brief. Specifically, the Examiner's Answer cites to new portions of the art of record. This Reply Brief responds to these new excerpts from the art of record.

Independent Claim 13

At p. 17, the Examiner's Answer presents new grounds of rejection for claim 13. Specifically, the Examiner contends that U.S. Patent No. 6,119,185 to Westerinen et al. ("Westerinen") at Col. 8, lines 38-51 teaches Applicants' claimed "with respect to the number of devices at the ports, assigning resources to the ports". Applicants respectfully disagree.

This excerpt of Westerinen, which is quoted in the Examiner's Answer, teaches that, where two computer resources are dependent upon each other, such as an interrupt queue and a memory address range, then during the process of assigning such resources to the devices of a computer the two inter-dependent resources should both be assigned at the same time. Otherwise, if only one resource is assigned, then according to Westerinen the second resource may for all practical purposes be rendered unavailable, and thus wasted.

Claim 13, in contrast, recites assigning resources to the ports **with regard to the number of devices at those ports**. Nothing in the newly cited excerpt from Westerinen teaches or suggests this limitation. For example, there is no mention by Westerinen for assigning resources as a function of the number of devices at the ports. Instead, the ex-

cerpt from Westerinen is focused solely on the particular resources being assigned, and the fact that two of the resources being assigned are dependent upon each other.

Accordingly, Applicants respectfully submit that claim 13 is distinguishable over the art of record, including the newly cited excerpt from Westerinen.

Dependent Claims 14, 16 and 31

At p. 18, the Examiner's Answer presents new grounds of rejection for claims 14, 16 and 31. Specifically, the Examiner's Answer cites to U.S. Patent No. 6,219,734 to Wallach et al. ("Wallach") at Col. 9, lines 13-26 as purportedly teaching Applicants' claimed assigning control registers to the ports. Applicants respectfully disagree.

This excerpt from Wallach is quoted in the Examiner's Answer. As shown, the excerpt states that Wallach's "configuration manager 500 also allocates resources for every managed adapter and **initializes each managed adapter's registers** during a hot swap operation." (emphasis added) That is, the excerpt teaches that the configuration manager 500 loads data values into the already existing registers at the adapters. The values loaded into these existing registers, moreover, cause certain actions to be carried out by the adapter, or indicate the status of the adapter. See Col. 9, lines 22-25 ("The registers of an adapter 310 are components or intermediate memories whose values issues (sic) a certain action in the adapter, or whose values indicate the status of the adapter.")

In contrast, claims 14, 16 and 31 each recite **assigning** control registers to the ports. Nothing in the newly cited excerpt from Wallach teaches or suggests that registers can be assigned to adapters. Instead, the excerpt notes that the data values contained in already existing registers can be modified to cause certain actions to be performed or to

change the status of the adapters. Accordingly, Applicants submit that claims 14, 16 and 31 are distinguishable from the art of record, including the newly cited excerpt from Wallach.

Independent Claim 32

At p. 20, the Examiner's Answer presents a new ground of rejection for claim 32. Specifically, the Examiner's Answer cites to Westerinen at Col. 10, line 65 to Col. 11, line 11 as purportedly teaching Applicants' claimed "programmable logic configured and arranged to assign the resources among the I/O ports in response to the number of I/O devices with which the I/O ports are communicating." Applicants respectfully disagree.

This excerpt from Westerinen, which is quoted in the Examiner's Answer, describes a process for assigning memory to requesting devices of a computer system. According to Westerinen's process, those devices requesting memory are organized into a list, and investigated individually. Specifically, a given device is investigated for a setting conflict, and a determination is made whether any ranked memory settings are available. If so, the device is assigned the highest ranking memory setting then available.

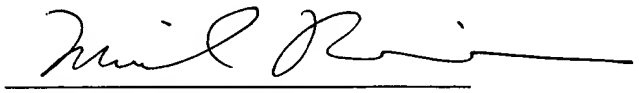
As shown, this newly cited excerpt from Westerinen provides no teaching or suggestion for the assigning of resources among I/O ports based on the number of I/O devices with which the I/O ports are communicating. Indeed, there is no mention at all in this excerpt about determining or considering the number of I/O devices that a given I/O port is communicating with. Accordingly, Applicants submit that claim 32 is distinguishable from the art of record, including the newly cited excerpt from Westerinen.

CONCLUSION

Applicants respectfully submit that the claims are allowable over the art of record.

Accordingly, Applicants request that the rejection of all claims be reversed.

Respectfully submitted,



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